



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Takao Myono et al.
Serial No. : 10/823,004
Filed : April 13, 2004
Title : CHARGE PUMP CIRCUIT

Art Unit : Unknown
Examiner : Unknown

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicant submits the references listed on the attached form PTO-1449.

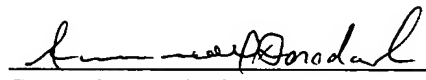
Item AA on the enclosed list is an English-language equivalent of item AL. An English-language abstract for item AL also is enclosed.

This statement is being filed before the receipt of a first Office action on the merits.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 7/30/04


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I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 14699-019001	Application No. 10/823,004
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Takao Myono et al.	
		Filing Date April 13, 2004	Group Art Unit

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	6,515,535	02/04/2003	Myono			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Abstract	
							Yes	No
	AL	2001-286125	10/12/2001	Japan			X	
	AM							
	AN							
	AO							
	AP							

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AQ	J. F. Dickson, "On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique", IEEE Journal of Solid-State Circuits pp 374-378 (1976)
	AR	
	AS	
	AT	

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	